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Original Research Article

Two-Dimensional Physical and Numerical Modelling of Copper (II)-Oxide/Silicon Hetero Junction Bipolar Transistor

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ABSTRACT

Flexible and printed electronics have been widely applied due to their low cost, scalability in manufacturing, and usability in biosensors as well as wearable electronics. However, there are some limitations on fabrication of these devices including thermal limitations. Thermal constraints are of significance since ion implantation at high temperatures is one of the most important stages of fabrication; therefore, despite these limitations, fabrication of flexible BJT is practically impossible through conventional methods. In this study, copper oxide was used for the collector and emitter area of Double Heterojunction Bipolar Transistor (DHBT) due to the low-temperature deposition of copper oxide through the printing method, and the ability to adjust the doping according to the deposition conditions. DC and high-frequency specifications of two transistors with PNP and NPN structures were simulated using two-dimensional semiconductor simulator atlas module of SILVACO software.

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1. INTRODUCTION

Flexible and printed electronics are of great importance in manufacturing and development of wearable devices [1-6], large solar cells [7-11], touch screens [12-13], and implantable circuits [14-15]. Several characteristics of these electronics have led to their development and wide applicability such as their ability to bend, non-breakable features, manufacturable roll-to-roll, and a large area. In printed and flexible electronics, transistor fabrication methods mostly require some steps such as different dopant introduction as well as annealing steps; these steps are not compatible with flexible and organic substrates [16-17], which may damage the organic substrate and negatively affect the device performance. In this regard, semiconductor metal oxides were employed to remove the ion implantation step and combine it with the deposition step. Among semiconductor metal oxides, copper oxide can be a good candidate for transistor fabrication. Copper oxide has some features such as low price, abundance in nature, easy deposition, and relatively large bandgap [18-23]. Among all of these features, the most important ones, which are also the main focus of this study, are the tunability of the bandgap and doping of impurities due to deposition condition [24,25]; these two factors can be

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adjusted during the deposition of copper oxide. So far, many copper oxide-based flexible transistors have been introduced that were of TFT type with a copper oxide channel [26-32]. Through the incorporation of copper oxide-based HBTs to flexible electronic circuits, the resultant material can be widely applied in wearable electronics, medical implants, and medical diagnostics.

The main objective of the present study was to investigate two different PNP and NPN structures based on CuO/Si heterojunction, simulate them based on the reported properties, and evaluate and compare the results of high-frequency and DC analysis of these two HBTs.

2. DEVICE STRUCTURES

In p-CuO/n-Si/p-CuO Heterojunction Bipolar Transistor (HBT), labeled as Device A, the structure layers consist of three layers including 0.1 µm, $p^+ = 10^{19}$ cm^{-3} CuO emitter layer; 0.1 µm, $n^+ = 10^{19}$ cm^{-3} Si base layer; and 0.8 µm, $p^+ = 10^{19}$ cm^{-3} CuO collector layer. Similar to the above structure, for NPN HBT, the structure layers consist of 0.1 µm, $n^+ = 10^{19}$ cm^{-3} CuO emitter layer; 0.1 µm, $p^+ = 10^{19}$ cm^{-3} Si base layer; 0.8 µm, $n^+ = 10^{19}$ cm^{-3} CuO collector layer, which is labeled as Device B. The dimensions of the areas of the emitter and collector areas are 0.1×0.8 and 2×0.8 μm^2, respectively. Also the semiconductor parameters were simulated based on the data detailed in Table 1.

TABLE 1. Parameters of CuO, Cu_2O and Si [25]

Parameter	CuO	Cu_2O	Si
Hole Mobility (cm^2/Vs)	5	80	≤450
Band Gap Energy (eV)	1.5	2.3	1.12
Electron Affinity (eV)	4.07	3.2	4.05
VB Effective Density of State (cm^{-3})	5×10^{18}	1.1×10^{19}	1.83×10^{19}
CB Effective Density of State (cm^{-3})	3×10^{19}	2.02×10^{17}	2.82×10^{19}
Carrier Lifetime (s)	212×10^{-12}	10^{-9}	10^{-7}
Dielectric Relative Permittivity	18.1	7.11	11.8

A two-dimensional semiconductor simulation package SILVACO was employed to analyze the energy band diagrams, carrier distributions, dc, and high-frequency performance. The simulated analysis takes into account Poisson's equation, continuity equation of electrons and holes, Shockley–Read–Hall (SRH) recombination, bandgap narrowing (BGN), Auger recombination, Concentration Dependent (CONMOB), Parallel Electric Field Dependence (FLDMOB), and Boltzmann statistics.

The schematic drawing of the device simulated is shown in Figure 1.

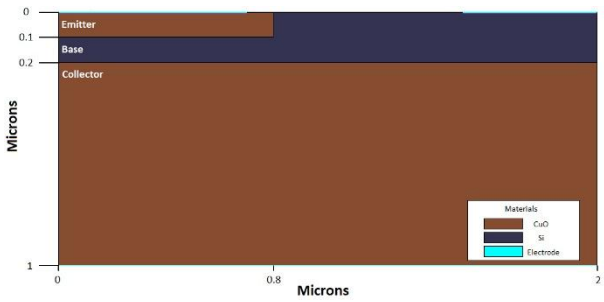

Figure 1. Schematic diagram of the simulated device

3. RESULTS AND DISCUSSION

3.1. Device A (PNP Structure)

The diagram of the energy band in the thermal equilibrium mode of device A is shown in Figure 2.

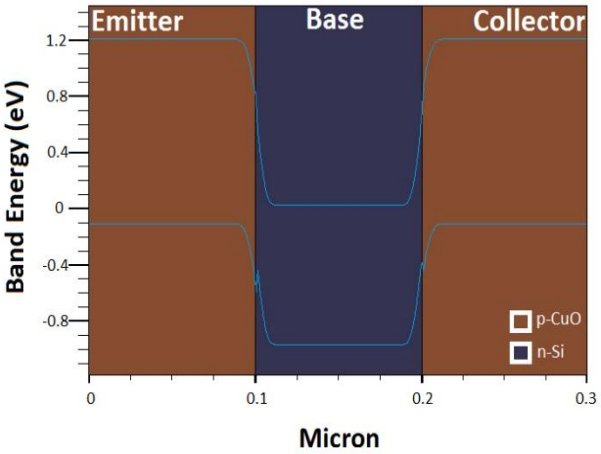

Figure 2. Energy band diagram of device A in the thermal equilibrium mode

The valence bands of the B-E and B-C junctions of the device A have spike potentials of 0.16 eV and 0.08 eV, respectively. One of the major problems with Heterojunction Bipolar Transistors (HBTs) is the presence of spike potential at the junctions and in their valence and conduction bands. Spike potential increases the turn-on voltage at the B-E and B-C junctions, resulting in offset voltage [33]. However, in DHBTs studied in this paper, due to the use of silicon copper-oxide bonds, compared to other HBTs, it has less spike potential.

$\alpha_0 = I_{CP}/I_E$

$$\alpha_0 = I_{Cp} / I_{Ep}+I_{En} = (I_{Ep} / (I_{Ep}+I_{En})) (I_{CP} / I_{Ep}) \quad (1)$$

The first part of the equation is called the efficiency of the emitter, which is actually the ratio of the injected holes to the total current of the emitter. For an ideal design, we want the efficiency of the emitter to be close to one; thus, I_{En} must be about zero.

The conduction band potential barrier prevents the injection of electrons from the base into the emitter. According to Equation (1), this is the main reason for the efficiency of the emitter and, as a result, the increase in current gain.

The collector current according to the collector voltage diagram of device A is shown in Figure 3. The turn-on voltage is 0.23 V.

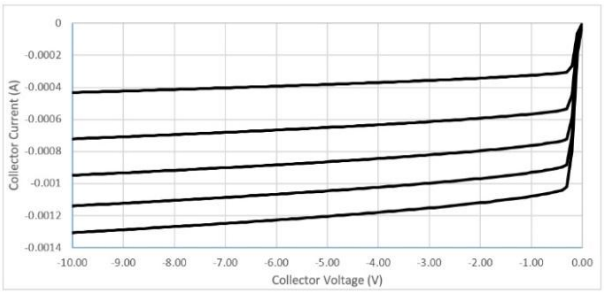

Figure 3. Current-voltage characteristic of the common bias emitter of device A with the base current step being 1 µA from zero

Figure 4 shows the zoomed image of the current-voltage characteristic in the common-emitter bias of the device A. The offset voltage is defined as the voltage that must be applied at the input to make the output zero. The offset voltage obtained for the base voltage of a microampere for this device is 9 mV. In general, the offset voltage in HBTs is due to the difference in the turn-on voltage between the B-E junction and the B-C junction. The higher the spike potential within the valance band of the device A, the higher the turn-on voltage will be. Using the quasi-symmetrical structure, the offset voltage problem in HBTs can be solved to some extent, the cause of which is discussed below. According to the diagram of the drawn energy band (Figure 2) for device A, there will be a spike potential in the valance band on both B-E and B-C junctions, thus increasing the turn-on voltage in both heterojunction bonds. However, the total offset voltage of the transistor which is the result of the potential difference between the B-E and B-C junctions is still small.

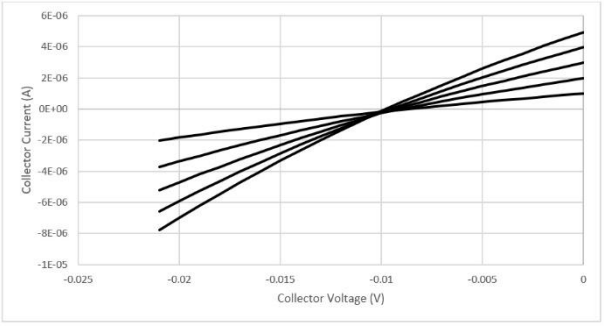

Figure 4. Zooming image of the current-voltage characteristic in the common bias emitter of device A, with the base current step being 1µA from zero

The electrical characteristics of the base current and the collector current as a function of forwarding bias are referred to as the Gummel plot, The Gummel plot of device A for collector currents and base currents is plotted according to Figure 5. The current amplification factor of device A is around 227 at base voltage of 0.7 V, and the ideality factor of diode according to base voltage of 0.7 V for collector current is 1.01 and for base current is 1.5, which indicates the predominance of diffusion and thermionic mechanisms of carrier motion. Also, according to the Gummel plot, when the base-emitter voltage is 0.7 V, the base recombination current does not prevail, thus reducing the ideal factor of diode of base current.

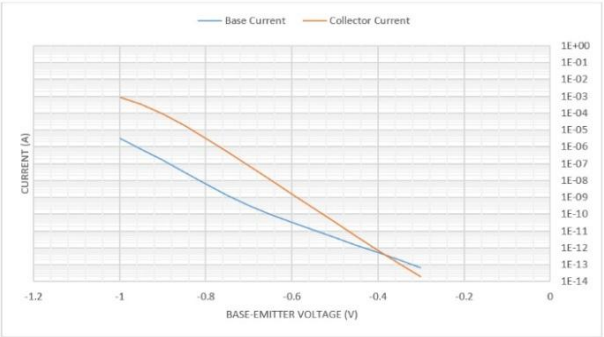

Figure 5. The Gummel plot for base and collector currents of device A while V_{CE} = -2 V

Figure 6 shows the relationship between current gain and operating frequency of device A. The unity gain cut-off frequency ft for this device is 10 GHz for VCE = 1 V. Figure 6 shows the AC gain of device A equal to 44 dB.

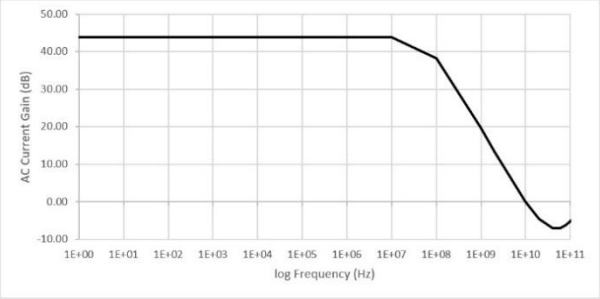

Figure 6. Current gain cut-off frequency (ft) of device A

3.2. Device B (NPN structure)

Now, in order to increase the gain of device A, device B is examined. In device B, the potential barrier of a majority of carriers in the base is greater and as a result, the gain is promoted.

The energy band diagram in thermal equilibrium is shown in Figure 7. Device B in its base-emitter junction conduction band has a spike potential of 0.04 eV, which is a very small value. Spike potential in the conduction band of the base-collector junction area is not given in Figure 7. Without the use of spike reduction techniques such as adding layers of different semiconductors between base-emitter and base-collector, these values are obtained which reduce the cost of manufacturing this transistor. Because the forbidden band of the emitter is larger than the base, a barrier is created in device B that prevents the entry of injection holes from the base to the emitter, thus increasing the current gain.

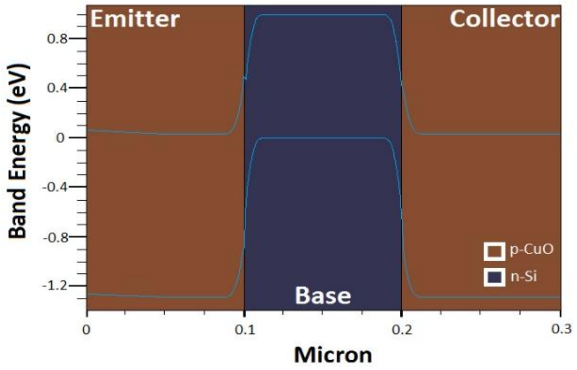

Figure 7. Energy band diagram of device B in thermal equilibrium.

The characteristic curve of the collector current according to the collector voltage of device B is shown in Figure 8. VBCEO = 5.8 V and the current base scale is one µA. The turn-on voltage for device B is 0.28 V according to Figure 8.

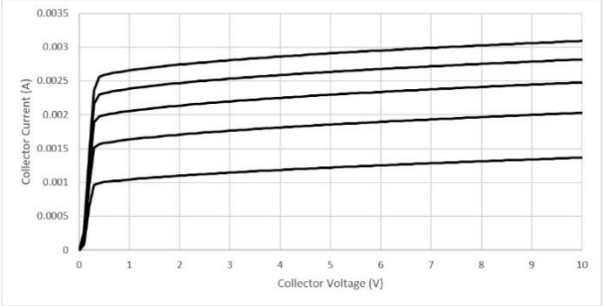

Figure 8. Voltage-current characteristic curve in the common bias emitter of device B, with the base current step being 1µA from zero

Figure 9 shows the zoomed image of the voltage-current characteristic curve of the common-emitter of the B device. The offset voltage obtained according to the base voltage of 1 µA for this device is 9 mV. In general, the offset voltage in HBTs is due to the difference in the turn-on voltage of B-E and B-C junctions.

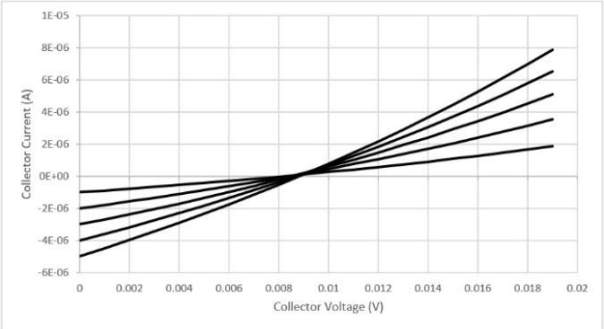

Figure 9. Zoomed image of Voltage-current characteristic curve in the common bias emitter of the device B, with the base current step being 1µA from zero.

The Gummel plot of device B for collector current and base current is plotted according to Figure 10. The current amplification factor of device B is around 578 at base voltage of 0.7 V, and the ideality factor of diode according to base voltage of 0.7 V for collector current is 1.01 and for base current is 1.33, which indicates the predominance of diffusion and Thermionic mechanisms of carrier motion. Also, according to the Gummel plot, when the base-emitter voltage is 0.7 V, the base recombination current does not prevail, thus reducing the ideality factor of base emitter diode.

Figure 11 shows the relationship between current gain and operating frequency of device B. The unity gain cut-off frequency ft for this device is 10 GHz for VCE = 1 V. Figure 11 shows the AC gain of device B, which is equal to 60.5 dB.

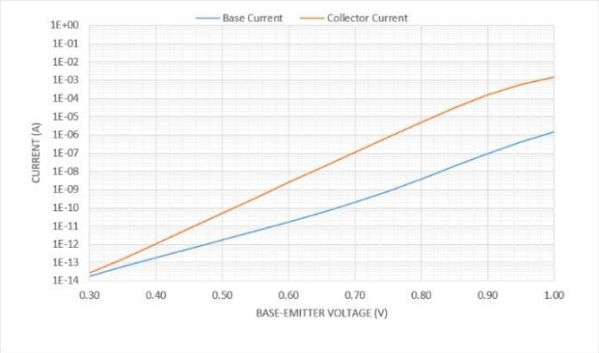

Figure 10. The Gummel plot for base and collector currents of device B while VCE=2V

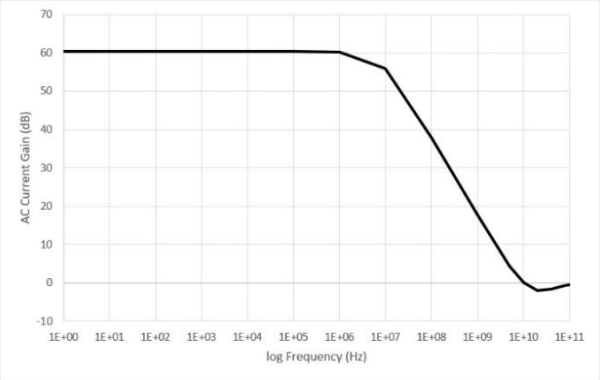

Figure 11. Current gain cut off frequency (ft) of device B

4. CONCLUSION

The physical model of two heterojunction bipolar transistors based on CuO/Si junction with PNP and NPN structures was investigated. Successful simulations of two HBTs using copper oxide semiconductors as emitter and collector regions and silicon for the base layer with excellent properties were presented and a high current gain factor was exhibited. The simulation results showed that there was a small spike potential in the base-emitter junction of both structures, which reduced the offset voltage of both transistors. The offset voltage obtained from these structures was acceptable even without the use of the emitter-base junction grading technique. This feature makes the use of this type of transistor in switching and driver circuits also applicable. In Device B, due to the presence of a potential barrier in the valance band, the base holes are prevented from entering the emitter, thus increasing the emitting efficiency and the DC and high-frequency current amplification. Given the existence of different methods of copper oxide deposition, there are different optical and electrical ranges such as energy band gap and density of carriers that can be researched to obtain the best electrical properties for different applications of bipolar transistors. Consequently, these structures can provide a wide range of applications in flexible circuits.

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